Amendments to the Claims

1. (currently amended) A method for fabricating an integrated circuit, comprising the steps of:

forming a low-k dielectric layer over a semiconductor body;

treating said low-k dielectric layer with a reducing plasma;

B1 treating said low-k dielectric layer with a wet solution;

forming a resist pattern over said low-k dielectric layer; ~~and~~

etching said low-k dielectric layer using said resist pattern; and

treating said low-k dielectric layer to a H_2 plasma after said step of treating said low-k dielectric layer with a wet solution and prior to forming said resist pattern.

2. (original) The method of claim 1, wherein said reducing plasma comprises H_2 and N_2.

3. (cancelled).

4. (original) The method of claim 1, wherein said wet solution comprises HF.

5. (cancelled).

6. (original) The method of claim 1, wherein said wet solution comprises a solvent.

7. (cancelled).

8. (cancelled).

9. (original) The method of claim 1, wherein said low-k dielectric layer comprises organo-silicate glass.

10. (original) The method of claim 1, wherein said treating step occurs prior to forming said resist pattern.

11. (original) The method of claim 1, wherein said treating step removes said resist pattern as a pattern re-work step.

B1 Cont.

12. (original) A method of fabricating an integrated circuit having copper metal interconnects, comprising the steps of:

forming an interlevel dielectric (ILD) over a semiconductor body;
forming an intrametal dielectric (IMD) over the ILD;
plasma treating said IMD using H_2 and an inert gas;
treating said IMD using a wet solution after said plasma treating step;
forming a via resist pattern over said IMD;
etching a via in said IMD and ILD using said via resist pattern;
removing said via resist pattern;
at least partially filling said via with a material;
forming a trench resist pattern over said IMD;
etching a trench in said IMD using said trench resist pattern;
removing said trench resist pattern and said material in said via; and
forming a copper interconnect in said via and said trench.

13. (original) The method of claim 12, wherein said inert gas comprises Ar.

14. (original) The method of claim 12, wherein said inert gas comprises N_2.

15. (original) The method of claim 12, wherein said wet solution is selected from the group consisting of HF, organic acid, HF combined with citric acid, solvent, and H_2SO_4.

16. (original) The method of claim 12, wherein said plasma treating step and said treating step occur prior to the step of forming the via resist pattern.

17. (original) The method of claim 12, wherein said plasma treating step occurs after the step of forming the via resist pattern as a pattern re-work step.

B1 Cont.

18. (original) The method of claim 12, further comprising the step of passivating said IMD using a H_2 plasma after said step of treating said IMD with a wet solution and prior to said step of etching a via.

19. (original) The method of claim 12, wherein said plasma treating step and said treating step occur after the step of removing the via resist pattern and prior to the step of forming the trench resist pattern.

20. (new) A method for fabricating an integrated circuit, comprising the steps of:

forming a low-k dielectric layer over a semiconductor body;

treating said low-k dielectric layer with a reducing plasma, wherein said reducing plasma comprises a H_2 and Ar;

treating said low-k dielectric layer with a wet solution;

forming a resist pattern over said low-k dielectric layer; and

etching said low-k dielectric layer using said resist pattern.

21. (new) A method for fabricating an integrated circuit, comprising the steps of:

forming a low-k dielectric layer over a semiconductor body;

treating said low-k dielectric layer with a reducing plasma;

treating said low-k dielectric layer with a wet solution, wherein said wet solution comprises an organic acid selected from the group consisting of citric, acetic, gallic, and oxallic;

forming a resist pattern over said low-k dielectric layer; and

etching said low-k dielectric layer using said resist pattern.

22. (new) A method for fabricating an integrated circuit, comprising the steps of:

forming a low-k dielectric layer over a semiconductor body;

B1 treating said low-k dielectric layer with a reducing plasma;

treating said low-k dielectric layer with a wet solution, wherein said wet solution comprises H_2SO_4;

forming a resist pattern over said low-k dielectric layer; and

etching said low-k dielectric layer using said resist pattern.